Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-24 (Canceled).

25. (Previously presented) A semiconductor device package, comprising:

a semiconductor device having diced edges;

a dielectric substrate having diced edges;

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a metal layer formed between said semiconductor device and said dielectric substrate, said metal layer having diced edges;

a ball grid array on said dielectric substrate, said dielectric substrate and said metal layer being located between said semiconductor device and said ball grid array; and

electrical connections between said semiconductor device and said ball grid array,

wherein said metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said metal layer edges, so as to provide said package with aligned edges.

26. (Original) The package of claim 25, wherein said metal layer provides a ground plane for said electrical connections.

Claim 27 (Canceled).

28. (Original) The package of claim 25, wherein said metal layer is arranged to dissipate heat from said semiconductor device.

29. (Original) The package of claim 25, wherein said metal layer comprises copper.

30. (Previously presented) The package of claim 25, wherein said connections comprise wire bonds.

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31. (Original) The package of claim 25, wherein said connections comprise conductive vias.

32. (Original) The package of claim 31, wherein said connections further comprise conductive traces on opposite sides of said substrate.

33. (Original) The package of claim 32, further comprising solder bumps on said semiconductor device, said bumps being connected to said traces.

34. (Previously presented) The package of claim 25, further comprising an insulative solder mask for covering said dielectric substrate.

Claims 35-38 (Canceled).

39. (New) The package of claim 25, wherein the metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

40. (New) A semiconductor device package, comprising:

a semiconductor device having diced edges;

a dielectric substrate having diced edges over an upper side of said semiconductor device;

a first metal layer having diced edges below a lower side of said semiconductor device;

a ball grid array over said dielectric substrate and on an opposite side of said dielectric substrate than said semiconductor device; and

electrical connections between said semiconductor device and said ball grid array.

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41. (New) The semiconductor package of claim 40, wherein said first metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said first metal layer edges, so as to provide said package with aligned edges.

42. (New) The semiconductor package of claim 40, wherein said first metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

43. (New) The semiconductor package of claim 40, further comprising a second metal layer below a lower side of said first metal layer and on an opposite side of said first metal layer from said semiconductor device.

44. (New) The semiconductor package of claim 43, wherein said first metal layer has a thickness of about 0.00254 millimeters.

45. (New) The semiconductor package of claim 43, wherein said second metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

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46. (New) The semiconductor package of claim 43, wherein the second metal layer has diced edges aligned with edges of said first metal layer, said semiconductor device edges, and said dielectric substrate edges.